WAYS TO INCREASE SPEED IN LARGE-COUNT BINARY COUNTERS*

by Jack Irwin

I INTRODUCTION

Hardware for large-count binary counters can be implemented using any of several methods. These methods vary in the required number of elements used and speed of operation. This application note considers what can be done to achieve higher speed of operation. Examples shown use Fairchild Micrologic® elements.

II DESCRIPTION

What Is "Large-Count"?

The definition of "large-count" binary counters is somewhat arbitrary. The main reason for this is that "largeness of count" is a function of the desired speed of operation. What may be a reasonably low count for a slow system could be a prohibitively large count for a fast system. The best way to approach the problem is to assume a case and look at it. For this discussion we have assumed the need for a 16-stage binary counter.

The Problem

The JK flip-flop triggers on a negative-going input transition. Normal operation in a ripple carry configuration would find the trigger coming from the "0" side of the preceding stage. Therefore, the time for a signal to reach the new state can be calculated by the following formula:

$$t_{delay} = n\,(t^-) + t^+$$

where n equals the number of stages going false. The additional time is for the next stage to go true. In this instance the "0" side is going positive, preventing further stages from triggering. The next stage will have its "1" side low in one more t^- time; however, the "0" side will not be up for a t^+ time.

The t^- and t^+ figures for the 923 JK are 25 nsec each. Thus, for the 16-stage ripple carry counter, one can expect a time of 400 nsec for the delay of all stages (16 x 25 nsec). Figure 1 shows five stages connected in this configuration. Using this method, one would need a minimum of 400 nsec or 2.5-Mc maximum clock rate for the 16 stages. Therefore, a higher frequency of operation must utilize techniques to reduce the total delay.

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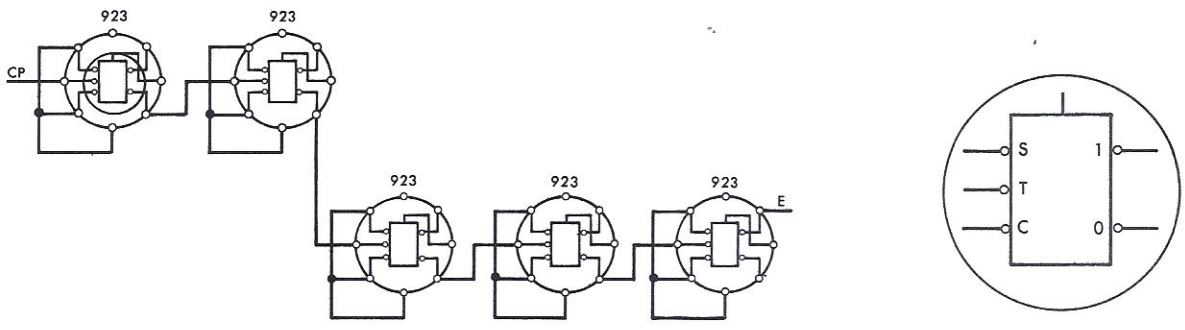

Fig. 1. Ripple counter

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III SPEEDUP TECHNIQUES

Parallel Gating All Stages

One technique is to use parallel gating on the inputs to the JK's (see Fig. 2). The JK flip-flop has the property that, with both inputs low at the change from positive to low voltage at the trigger input, the output changes state. It then is possible to put the input clock on the trigger pin of all the JK's. The set and clear pins would be connected to an AND function of all preceding flip-flops. Thus it can be seen that the delay of even the final stage is only that through one JK stage, with the requirement that there be time for the signals from the lower stages to propagate through the gating with sufficient set-up time for the JK.

The limiting factor for this method is the amount of hardware needed. The resulting hardware comes from two points. The first is the gating for each stage, which requires one additional input per stage. Thus, the set and clear inputs to the first stage are grounded. The inputs to the second stage are tied to the true term of the first stage. The inputs to the third stage are the inverted AND functions of the first and second stage (inverting RTL logic is used). The inverted AND functions of the first three stages provide the signal to the control inputs of the fourth stage. This procedure is followed for each successive stage.

The resulting hardware is 1/2 of a 914 dual two-input gate and one inverter from the 927 quad inverter element for the gating into the third stage. The gating for the fourth stage would be a three-input gate and an inverter. The fifth stage gating would be a four-input gate and an inverter. The sixth stage gating would be a combination gate to give five inputs (an inverter and a four-input gate) and an inverter. In all cases of combinations of gates where outputs are tied together, only one gate may have V_{CC} connected. Totaling these requirements results in twenty-four 907's, two 914's, two 915's, and five (4-1/4) 927's for the gating.

The second source of hardware is the loading. Using μL loading rules (base load factor equal to one), the JK has a fan-out of three. Hence, the first 12 stages must have additional fan-out. This can be done best by using inverters off of the "0" side of the flip-flop. The loading requires an additional five 927 (quad inverter) elements. In addition, another 900 buffer is required to help drive the clock line. Therefore, 39 additional elements are needed to do the parallel-gated version. Figure 2 shows the first five stages of this method.

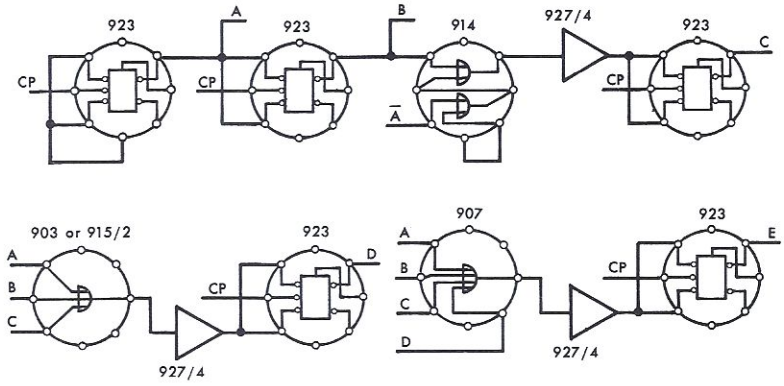

Fig. 2. Parallel counter

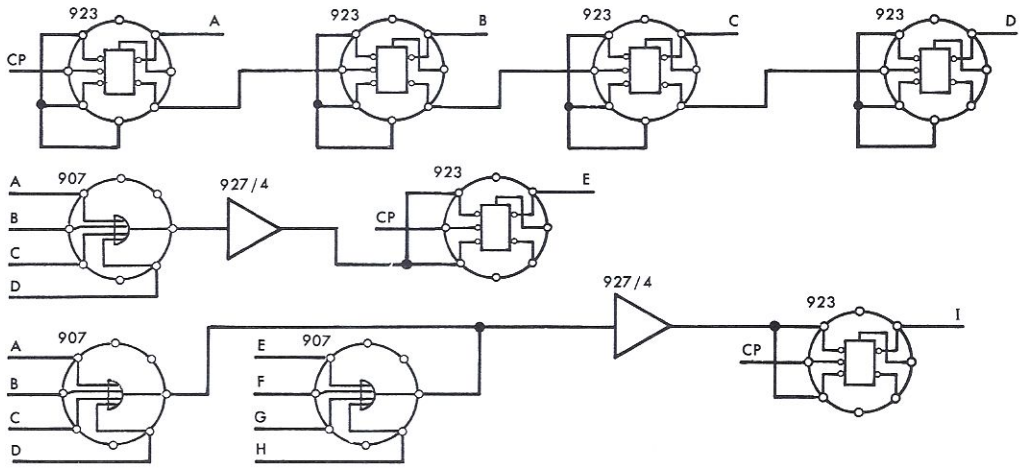

Fig. 3. Parallel-by-four counter

Parallel Gating Some Stages

A compromise, between element count and speed, can be reached by clocking and gating only part of the stages. As an example, every fourth stage could be gated. Then only seven (6-3/4) devices are needed for the 16-stage counter, as a result of reducing both gating and loading. This circuit was built up and, running at 10 Mc, had a worst-case delay of 80 nsec. Figure 3 shows the first group of four and the inverted AND signal into the fifth stage.

The optimized point between speed and element count would determine the number of stages between gating for a particular application. Thus it might be that for a particular system, gating every eight stages would be sufficient for the desired speed and would reduce the element count.

Series Connection of Signals

Another method would be a series connection of the signals. In this technique, from the third stage on, the subsequent stages are ANDed with the inverted gating signal that "enables" that stage. As an example, the first stage enables the second. The first and second stage are ANDed and inverted to enable the third stage. The third stage is then ANDed with its enabling signal. This signal inverted enables the fourth stage, etc. While this example is for gating and clocking each stage, it could be done for every second, fourth, or desired stage. Figure 4 shows five stages of a series connection by two, while Fig. 5 shows five stages of a series connection by four.

This method is more susceptible to decoding spikes. However, one may AND the clock pulse (inverted) into the AND circuitry and eliminate these spikes.

The serial method is inherently slower than the parallel methods described earlier because the signals go through more gates. However, as the number of stages between gating goes up, the over-all delay from the gating comes down, since there are fewer stages for the gating signal to go through.

Gating With Low-Power Devices

Another consideration in all of the schemes is the use of the low-power family of devices for gating. Although these devices are inherently slower, their reduced loading at times will save in the number of driving inverters needed and the delay resulting from them.

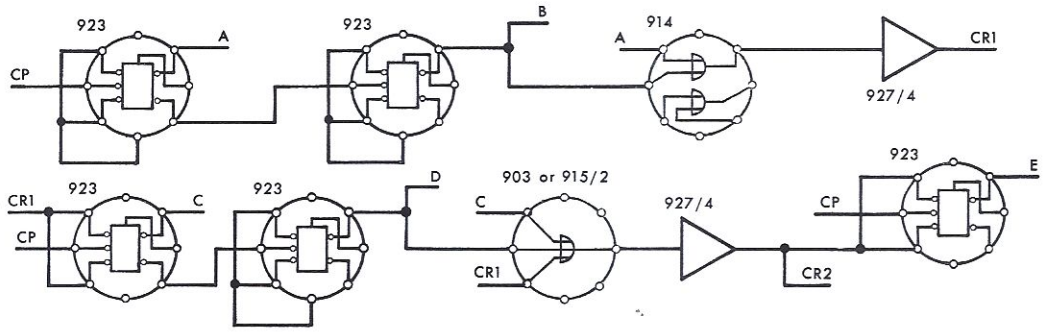

Fig. 4. Series-parallel-by-two counter

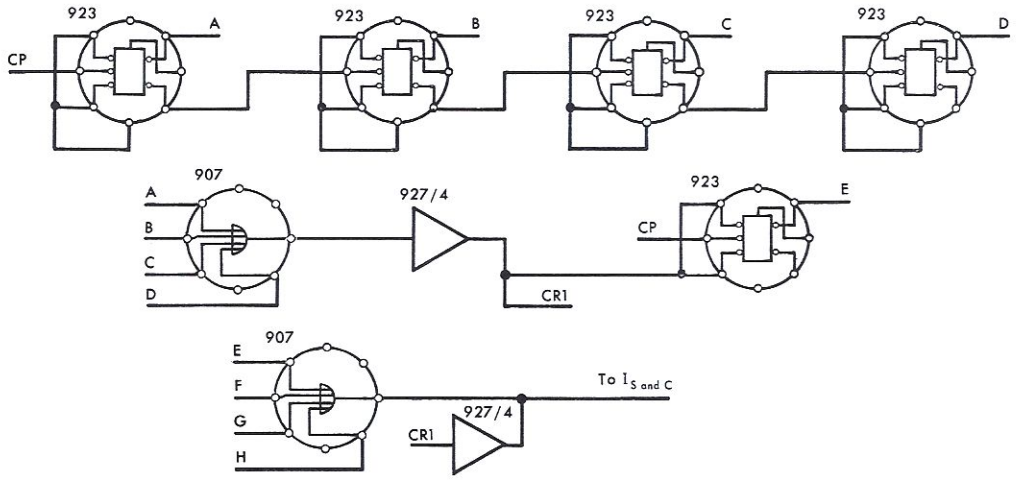

Fig. 5. Series-parallel-by-four counter